24. The method of claim 23 wherein the porous silicon oxide layer fills the at least one gap.

25. A method for forming an insulation layer over a substrate having at least one gap, the method comprising:

forming a surface sensitive silicon oxide layer over the substrate partially filling the at least one gap; and

forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400°C or less.

26. The method of claim 25 wherein the porous silicon oxide layer fills the at least one gap.

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REMARKS

Claims 1-26 are pending. Claim 1 has been amended to more particularly point out and distinctly claim Applicants' invention. New claims 21-26 have been added. No new matter has been introduced. Applicants believe the claims comply with 35 U.S.C. § 112.

Claims 1-19

Claims 1, 2, 4-6, and 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Cho (USP 5,804,509).

Applicants respectfully submit that independent claim 1 is novel and patentable over Cho because, for instance, Cho does not disclose or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. This feature is discussed in the specification at page 17, lines 13-18.

Applicants note that Cho also fails to disclose, for example, that the porous silicon oxide layer has a carbon content of at least 5 atomic percent as recited in claim 2, and that the surface sensitive silicon oxide layer is deposited from a plasma enhanced CVD reaction of TEOS and oxygen as recited in claim 4.

For at least the foregoing reasons, claim 1 and claims 2, 4-6, and 9 depending therefrom are novel and patentable over Cho.

Claims 3, 7, 8, and 10-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho in view of Lan (USP 6,180,507). Lan is cited for allegedly disclosing that the porous silicon oxide layer has a dielectric constant lower than that of a conventional silicon oxide layer.

Applicants note that Lan fails to cure the deficiencies of Cho because, for instance, Lan does not teach or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min, as recited in claim 1 from which claims 3, 7, and 8 depend. Therefore, claims 3, 7, and 8 are patentable over Cho and Lan.

Applicants respectfully assert that independent claim 10 is patentable over Cho and Lan because, for instance, they do not teach or suggest depositing a plasma enhanced CVD silicon oxide layer over a plurality of conductive lines, and depositing a thermal silicon oxide layer over the plasma enhanced CVD silicon oxide layer. Cho and Lan also fail to disclose or suggest that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.

The Examiner alleges that Cho and Lan disclose plasma enhanced CVD silicon oxide layers, but Cho and Lan do not even mention plasma at all.

For at least the foregoing reasons, claim 10 and claims 11-19 depending therefrom are patentable over Cho and Lan.

New Claims 21-26

New claims 21 and 22 depend from claim 10, and are submitted to be patentable as being directed to additional features of the invention as well as by being dependent from allowable claim 10. Claim 21 recites that the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines. Claim 22 recites that the thermal silicon oxide layer fills the gaps between the plurality of conductive lines. The Examiner alleges that the first insulating layer (3) in Cho is the plasma enhanced CVD silicon oxide layer and the second insulating layer (4) is the

thermal silicon oxide layer. The first insulating layer (3) in Cho, however, fills the gaps, while the second insulating layer (4) is disposed above the gaps.

New claims 23 and 24 depend from claim 1, and recite additional features not taught or suggested in Cho and Lan. Claim 23 recites that the surface sensitive silicon oxide layer partially fills the at least one gap on the substrate. Claim 24 recites that the porous silicon oxide layer fills the at least one gap.

Applicants believe new claim 25 is patentable over the cited references because, for instance, they do not teach or suggest forming a surface sensitive silicon oxide layer over the substrate partially filling the at least one gap, and forming a porous silicon oxide layer on the surface sensitive silicon oxide layer. The references further fail to disclose or suggest that the porous silicon oxide layer fills the at least one gap, as recited in dependent claim 26.

Claim 20

Apparatus claim 20 is withdrawn from consideration pursuant to the restriction requirement. Claim 20 recites a substrate processing system comprising a memory having a computer-readable program that encompasses any and every computer implementation of the process as recited in the process claims.

MPEP § 806.05(e) states: "In applications claiming inventions in different statutory categories, only one-way distinctiveness is generally needed to support a restriction requirement." Specifically, if it can be shown "(A) that the process *as claimed* can be practiced by another and materially different apparatus or by hand, or (B) that the apparatus *as claimed* can be used to practice another materially different process", then restriction is proper. *Id.* (emphasis in original). MPEP § 806.05(e) further states: "If applicant proves or provides convincing argument that there is no material difference . . . , the burden is on the examiner to document another materially different process or apparatus or withdraw the requirement."

Applicants contend that the apparatus claim 20 is not materially distinct from the process claims (1-19) because the apparatus claims encompass any and every computer implementation of the process recited in the process claims, so that the

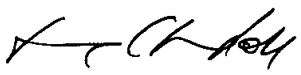
apparatus claim is to be examined on the basis of the underlying process. In the present case, apparatus claim 20 defines the physical characteristics of a computer or computer component exclusively as functions or steps to be performed on or by a computer, and encompasses any and every product in the state class (e.g., computer, computer-readable memory) configured in any manner to perform that process. In addition, the specification does not include specific software, i.e., programming code recited to define the aforementioned functions. As a result, the apparatus claim 20 and process claims (1-19) stand or fall together. Accordingly, Applicants respectfully request that the restriction requirement be withdrawn and that claim 20 be allowed.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claim 1; and add new claims 21-26 as follows.

1. (Amended) A method for forming an insulation layer over a substrate, the method comprising:

forming a surface sensitive silicon oxide layer over the substrate; and

forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400°C or less;

wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min.

New

~~21.~~ 21. The method of claim 10 wherein the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines.

22. The method of claim 21 wherein the thermal silicon oxide layer fills the gaps between the plurality of conductive lines.

23. The method of claim 1 wherein the substrate includes at least one gap, and wherein the surface sensitive silicon oxide layer partially fills the at least one gap.

24. The method of claim 23 wherein the porous silicon oxide layer fills the at least one gap.

25. A method for forming an insulation layer over a substrate having at least one gap, the method comprising:

forming a surface sensitive silicon oxide layer over the substrate partially filling the at least one gap; and

forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400°C or less.

26. The method of claim 25 wherein the porous silicon oxide layer fills the at least one gap.--